CLAIMS

What is claimed is:

1. An apparatus, comprising:

a circuit to generate a training pattern;

a debug circuit to generate debug information; and

an information assembly unit to combine the training pattern with the debug information.

2. The apparatus of claim 1, further comprising a serializer unit to serialize the combined debug and training pattern information.

3. The apparatus of claim 2, further comprising an output circuit to drive the combined debug and training pattern information onto an interconnect.

4. The apparatus of claim 3, the output circuit to drive the combined debug and training pattern information onto a high-speed asynchronous interconnect.

5. The apparatus of claim 4, the training pattern to include parity information.

6. The apparatus of claim 5, the serializer unit to reduce the debug and training pattern information down to 10 wires.

7. The apparatus of claim 6, the output circuit to output 10 bits at a time onto the interconnect.

8. The apparatus of claim 7, the debug and training pattern information organized into 80 bit packets, where 72 bits are debug information and 8 bits are training pattern information.

9. An apparatus, comprising:

an input circuit to receive combined debug and training pattern information over an interconnect; and

a de-serialization unit to receive the debug and training information from the input circuit; and

a data extraction unit coupled to the de-serialization unit to separate the debug information from the training pattern information.

10. The apparatus of claim 9, further comprising a buffer to receive the separated debug information from the data extraction unit.

11. The apparatus of claim 10, further comprising a memory controller coupled to the buffer, the memory controller to transmit the debug information over a memory bus.

12. The apparatus of claim 11, the input circuit to receive 10 bits at a time from the interconnect.

13. The apparatus of claim 12, the debug and training pattern information organized into 80 bit packets, wherein 72 bits are debug information and 8 bits are training pattern information.

14. A system, comprising:

a transmitting device including

a circuit to generate a training pattern,

a debug circuit to generate debug information,

an information assembly unit to combine the training pattern with the debug information, and

a serializer unit to serialize the combined debug and training pattern information; and

a receiving device coupled to the transmitting device via an interconnect, the receiving device including

an input circuit to receive the combined debug and training pattern information over an interconnect, and

a de-serialization unit to receive the debug and training information from the input circuit, and

a data extraction unit coupled to the de-serialization unit to separate the debug information from the training pattern information.

15. The system of claim 14, the transmitting device further including an output circuit to drive the combined debug and training pattern information onto the interconnect.

16. The system of claim 15, wherein the interconnect is a high-speed asynchronous interconnect.

17. The system of claim 16, the output circuit to output 10 bits at a time onto the interconnect.

18. The system of claim 17, the debug and training pattern information organized into 80 bit packets, where 72 bits are debug information and 8 bits are training pattern information.

19. A method, comprising:

combining debug information with a training pattern;

serializing the combined information; and

outputting the serialized debug and training information onto an interconnect.

20. The method of claim 19, wherein combining debug information with a training pattern includes combining debug information with a training pattern that includes parity information.

21. The method of claim 20, wherein serializing the combined information includes reducing the combined information down to 10 wires.

22. The method of claim 21, wherein outputting the serialized debug and training pattern information includes outputting 80 bit packets, wherein 72 bits are debug information and 8 bits are training pattern information.